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|---|
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| ART UNIT | PAPER NUMBER |
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| 2186 | 6 |

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/591,615 | SIX ET AL. | |
| | Examiner | Art Unit | |
| | Pierre-Michel Bataille | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is taken in response to applicant's communication filed June 17, 2003 in response to Official Action dated January 27, 2003. Applicant's amendments and/or arguments have been considered with the results that follow.

2. Claims 1-10 were originally presented in the application under examination. Of the original claims, claims 11 and 12 have been added; no claims have been canceled. Therefore, claims 1-12 are now pending in the applications.

### *Response to Arguments*

3. Applicant's arguments filed June 17, 2003 have been fully considered but they are not deemed to be persuasive for at least the following reasons that follow.

In view of the amendment to the specification, Objection noted in Section 2 of previous Action is withdrawn.

I. With respect to the rejection of claims 8-10 in view of US 5,638,530 (Pawate et al), applicant's references:

A. quoted section of Pawate showing that bus arbitration is required (4th full paragraph, page 5). This section acknowledged by Applicant corresponds to the claimed feature recited in claim 8: "sharing access to the memory circuit between the plurality of requestor circuits when the digital system is in a first

mode of operation". Pawate clearly teaches, as acknowledged by applicant, that arbitration is required for a DSP (digital signal processor) and a host computer to shared access of a memory device in a shared mode or standard mode [Col. 13, Lines 53-65; Col. 14, Lines 32-41].

B. argument that Pawate fails to teach or suggest, "selecting a first portion of memory in accordance with a size parameter and limiting access to the selected portion". In contrast, Pawate teaches the use of control registers for shared or standard mode and smart mode, the registers being accessed for control and mapping. Specifically, Col. 7 (Lines 8-30) quotes: "The operating mode, for example, the smart mode or the standard mode of the smart card is controlled by the control, status and communication registers. ... While in the smart mode, the first 2K bytes of the host computer (200) are not available to the host computer for shared memory access." Particularly, Col. 13 (Lines 53-56) of Pawate discloses: "The first kilobytes of the shared memory the host computer cannot access while the card is in the first mode. While in the smart mode, the host computer cannot access, by reading and writing, the first 2K bytes of the shared memory".

Pawate teaches, the recited access limiting of claim 8, as access to the first 2K bytes of the memory in smart access mode does not require arbitration because the host computer may not access any location within the noted memory range. The above quoted sections make the fact clear. Moreover, Col. 6, Line 59 to Col. 7, Line7, provides more clarification to the fact, reciting: "While the smart card (100) is in the smart mode, the DSP (170) is active and executes instruction code from either the common memory (150) or the attribute memory (160). The first 2K bytes, for example, of common memory are remapped into physical locations in the interface and controller circuit

(180). While in the smart mode, the DSP (170) communicates with the host computer (200) by a set of host communication registers. Thus, the host computer is able to access the communication registers in the shared memory and the operation of the DSP (170) continues since no bus arbitration is required while these registers are being accessed. The host computer (200) can parallel process while maintaining communication with the DSP (170). The host computer (200) may not access any other locations within this 2K byte block while the smart card (100) is in the smart mode since the result may be unpredictable."

C. argument that Pawate does not teach use of a control register that provides limited access and quoted a section in Pawate featuring that 'access to registers by host computer does not halt operations of the DSP since communication control and control registers are not resident in the shared memory'. Not only Pawate discloses, as required in the claims, the use of control registers to provide limiting access, the registers being accessed for control and mapping [see Col. 7, Lines 8-30], but also the claims do not require communication and control registers **be** resident in the shared memory, as argued by applicant. In contract to application assertion that the registers in Pawate are not shared, the paragraph of Col. 6, Line 59 to Col. 7, Line 7 shows that both the DSP and the host computer are able to access the communication registers in the shared memory.

II. With respect to applicant's argument pertaining to the rejection of claim 9, Pawate teaches the invention as claimed. Applicant is right by stating that Pawate teaches: "while the smart card is in the standard mode, the DSP is inactive... (Col. 6, lines 47-49). But, applicant fails to add that Pawate teaches, "the host computer always has

the higher priority for accessing the shared memory" (Col. 13, Lines 29-33) and "While in the smart mode, the host computer cannot access, by reading and writing, the first 2K bytes of the shared memory. Thus, these first two kilobytes of memory could be used as protected memory for the DSP. However, if the host computer accesses this protected block, the DSP is not put into a hold state." (Col.13, Lines 55-60). Clearly, access by the host processor to the first 2K bytes implies standard mode where arbitration is required and where the host computer is always assigned higher priority. If the first 2K bytes cannot be accessed by the host computer, the memory is in protected mode or smart mode. Respectfully, Col 13, line 30 recites: "... *smart card*, bus arbitration is necessary", in place of "smart mode", as stated by applicant.

III. With respect to applicant's argument pertaining to the rejection of claim 10, Pawate teaches the feature of the claim. Pawate teaches the DSP be maintained at reset while in smart mode to minimize power consumption of the smart card. Pawate meets the features of the claim because: the DSP, while in smart mode, is maintained in low power mode (Col. 9, Lines 53-56) and the DSP having exclusive access to the first 2K bytes in smart mode "allows the host computer to have quicker access to the remaining unused portion of the memory card" (Col. 9, Lines 6-11).

IV. With respect to applicant's argument pertaining to the rejection of claims 1-7, applicant argues neither Pawate (US 5,638,530) nor Boutaud (US 5,838,934) provides teaching or suggestion to select a first portion of memory in accordance with a size

parameter and to limit access to the selected portion. In contrast and as presented above, Pawate does provide such requirement.

Applicant admits that Boutaud does have a shared access mode (SAM) and a host only mode (HOM) and further argues that the entire memory is treated as a single portion used in either HOM or SAM. However, it is not uncommon to one, having ordinary skill in the art, to partition a memory and used each partition for distinct purposes. For example, Pawate teaches first 2K bytes (partition) of memory, in smart mode, not available to the host computer for shared memory access while in shared mode are accessed by the host computer and a DSP (Col. 13, Lines 53-56).

The January 2, 2003 Office action acknowledged that Pawate fails to show a selection circuit, but acknowledged that the selection feature would have been inherent in Pawate's disclosure as the first 2K bytes of memory are provided exclusive access by the DSP in smart mode of operation. The following provides fact for such inherency.

1. Pawate makes use of control registers to provide limiting access to the 2K bytes of memory accessible only by the DSP in smart mode (Col. 7, Lines 8-30). Pawate shows that the registers are shared and that both the DSP and the host computer are able to access the communication registers in the shared memory, and in response to accessing the registers, accesses to particular portions of the memory card are determined (Col. 6, Line 59 to Col. 7, Line 7). Therefore, since access to the registers provides control of the smart card such as selective access of the first 2K bytes, accessed exclusively or protectively by the DSP in smart mode while the host computer access is permitted access to the remaining memory portion, selection circuit coupled to the size register (control and communication registers in Pawate) is inherent.

2. Pawate teaches "The operating mode, for example, the smart mode or the standard mode of the smart card is controlled by the control, status and communication registers (110) ... (Col. 7, Lines 8-10) ... These registers are mapped into the first 2K bytes, for example (000000h-0007FFh), of the host computer to ensure that the host computer (200) will not accidentally change interrupt vectors of the DSP (170) interrupting the DSP (170) while the card (100) is in the smart mode. While in the smart mode, the first 2K bytes of the host computer (200) is not available to the host computer for shared memory access." (Col. 7, Lines 31-39). These quoted sections show clear selection of a first portion of the smart card in response to accessing the registers. Therefore, because selection circuit coupled to the registers, as required in the claims, is inherent in Pawate's disclosure, amendment to claim 1 does not carry any distinctive feature in view of the applied references.

V. With respect to claims 2-7, as shown above in Paragraph II-IV, Pawate discloses the feature of the claims, as shown in the rejection and as argued above.

VII. New claims 11-12 have been added. Rejection with respect to the claims is appended below.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,638,530 (Pawate et al).

With respect to claim 8, Pawate teaches a system and method operating a digital system having a memory circuit (*smart card*) that is shared by a plurality of requestors circuits (*digital signal processor 170 and host computer 200*) [Fig. 2] comprising: sharing access to the memory circuit (smart card) between the plurality of requestors circuits (*digital signal processor 170 and host computer 200*) when the digital system in a first mode of operation (*standard mode*) [Col. 13, Lines 53-65; Col. 14, Lines 32-41]; selecting a portion of the memory (*attribute memory 160 of the smart card*) responsive to a size parameter stored in a register (*interface configuration registers 130*) [Col. 4, Lines 53-65], such that the second portion is not selected (*common memory 150 of the smart card*) [Col. 7, Lines 36-42]; and limiting access (*smart mode*) to the first portion of the memory circuit (*attribute memory 160 of the smart card*) to only a first requestor (*digital signal processor (DSP) 170*) in a second mode of operation (smart mode) [Col. 13, Lines 53-65; Col. 14, Lines 32-41; Col. 7, Lines 22-42, Col. 7, Line 61 to Col. 8, Line 2].

With respect to claim 9, Pawate teaches sharing access to the second portion of the memory circuit between the plurality of requester circuits when the digital system is in the second mode of operation [Col. 13, Lines 53-65; Col. 14, Lines 32-41].

With respect to claim 10, Pawate teaches placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation *(minimizing power consumption of the smart card while in the smart mode until an external event, allowing the host computer to have quicker access to the remaining unused portion on the card)* [Col. 9, Lines 53-56; Col. 14, Lines 3-13].

With respect to claim 11, Pawate teaches the memory having a total size equal to the sum of the first portion and the second portion (the first 2K bytes (first portion) to be used exclusively by the DSP and memory pages (the remaining portion) can be desiccated exclusively for use by the host computer) [Col. 13, Lines 55-65].

With respect to claim 12, Pawate teaches storing a different size parameter in the register, such that the selection results in a first portion having a different size in response to different parameter [(use of the first 2K bytes is only exemplary (i.e. different size could be used) as the DSP can address up to 256M bytes of memory of 16 pages of 4MX32 each) Col. 6, Lines 22-40].

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,838,934 (Boutaud et al) in view of US 5,638,530 (Pawate et al)

With respect to claim 1, Pawate teaches a system and method operating a digital system having a memory circuit (*smart card*); a plurality of requestors circuits including first requester circuit with a first access node (*digital signal processor 170*) and a second requester circuit with a second access node (*host computer 200*) [Fig. 2]; a scheduling circuit (*PC/DSP bus arbitration circuit 120*) connected to the first access node and to the second access node operable to sequentially schedule memory access to the memory circuit by the first and second requester circuit [Col. 13, Lines 29-33; Col. 3, Lines 18-20]; and access mode circuitry for:

sharing access to the memory circuit (smart card) between the plurality of requestors circuits (*digital signal processor (DSP) 170 and host computer 200*) when the digital system in a first mode of operation (*standard mode*) [Col. 13, Lines 53-65; Col. 14, Lines 32-41];

selecting a portion of the memory (*attribute memory 160 of the smart card*) responsive to a size parameter stored in a register (*interface configuration registers 130*) [Col. 4, Lines 53-65], such that the second portion is not selected (*common memory 150 of the smart card*) [Col. 7, Lines 36-42]; and limiting access (*smart mode*) to the first portion of the memory circuit (*attribute memory 160 of the smart card*) to only a first requestor (*digital signal processor (DSP) 170*) in a second mode of operation (smart mode) [Col. 13, Lines 53-65; Col. 14, Lines 32-41; Col. 7, Lines 22-42, Col. 7, Line 61 to Col. 8, Line 2].

Pawate fails to specifically teach a selection circuit connected to the scheduling circuit request output node with an output node connected to the memory circuit. Although this features would be inherent in Pawate's disclosure (see Section IV, pp 5-7), Boutaud teaches a selection circuit (multiplexer 111, 113, 121, 123 and 160) connected to first memory access node (host port internal data and address 110 to mux (111, 113, 121, and 123) and control bus 138c to mux 160) and to a scheduling circuit request output node (synchronizer logic with output line 136, 146) with an output node connected to the memory circuit (output line 115c, 116c, 122a, 124a connected to the memory via memory interface logic 140, which provides the address, data and control via address, data and control line 148a, 148d, and 148c) [Col. 5, Lines 14-26; Col. 6, Lines 8-14]; wherein control logic is used to determine the type of access (Col. 10, Lines 48-51; Col. 8, Lines 28-31), shared access mode (SAM) or host only mode (HOM) (Col. 12, Lines 32-36) where control logic 130a generates memory control synchronous memory control signals when shared access mode is required (Col. 9, Lines 1-18)], such that both the first requester circuit and the second requester circuit can sequentially access the memory circuit when the priority circuitry indicates a first relative priority state between the first priority and the second priority (Col. 13, Lines 25-40); when in shared access mode (SAM) access by both the host 400 and the processor 300 are synchronized to clock signals to avoid conflicts (Col. 8, Lines 63-67; Col. 16, Lines 14-21; Col. 8, Lines 59-63: Col. 16, Lines 22-27].

Therefore, it would have been obvious to one having ordinary skill in the art and having both teaches before him at the time of the invention, to combine the selection feature of claim Boutaud with the digital signal processing system of Pawate because

the selection feature would have provided control using either synchronous or asynchronous clock signal to portion of the memory circuit for selectively providing selectively accessible by first type of requestor and second type of requestor, as taught by Boutaud Col. 2, Lines 18-31].

With respect to claim 2, Pawate teaches placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation *(minimizing power consumption of the smart card while in the smart mode until an external event, allowing the host computer to have quicker access to the remaining unused portion on the card)* [Col. 9, Lines 53-56; Col. 14, Lines 3-13].

With respect to claim 3, Pawate teaches the second portion of the memory circuit, not selected in response to the size parameter can be accessed by the second requester when the access mode indicates the second mode of access [Col. 13, Lines 53-65].

With respect to claim 4, Pawate teaches the indication of first access mode such that the entire memory is operable to be selected for sequential access by the first requester and the second requestor [Col. 13, Lines 29-48].

With respect to claim 5, Pawate teaches clock circuit connected to the DSP and the memory circuit wherein the first portion of the memory operates synchronously with the clock circuit in the first mode of access and wherein the first portion of the memory operated asynchronously in the second mode of access [Col. 13, Lines 62-65; Col. 14, Lines 2-42]; Boutaud additionally teaches sharing access to the memory circuit between the plurality of requestor circuits

(shared access mode (SAM Mode when in shared access mode (SAM), accesses by both the host 400 and the processor 300 are synchronized with clock signals and provided sequentially to avoid conflicts) [Col. 8, Lines 63-67; Col. 16, Lines 14-21] and limiting scheduling accesses to one of the requester with no need to synchronize host accesses with the processor clock signals (bypassing the synchronizer logic 130c in host only mode (HOM) Col. 8, Lines 59-63; Col. 16, Lines 22-27].

With respect to claims 6 and 7, Pawate teaches the system wherein the first requestor is a host processor and the second requester is a direct memory access circuit channel controller [Fig. 1]; and the system being a digital signal processing system comprising an integrated keyboard provided with keyboard adapter, a display, radio frequency and an aerial connected with the radio frequency [inherent in all cellular telephone; Fig. 1 and Fig. 2].

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,815,167 () teaching an interface arrangement for a shared memory having first and second memory portions, wherein shared access is provided to the first memory portion in a first state and exclusive access to the second memory portion when in a second state so as to facilitate exclusive access.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Pierre-Michel Bataille
Examiner
Art Unit 2186

July 25, 2003